DELAY-LOCKED LOOP WITH BUILT-IN SELF TEST OF PHASE MARGIN

ABSTRACT OF THE DISCLOSURE

A method and apparatus for measuring phase margin of a delay-locked loop (DLL) is provided in which a reference clock is applied to a reference input of the DLL. An auxiliary variable delay is coupled within the DLL and is varied until the DLL becomes unstable. A phase margin output is generated as a function of a value of the variable delay at which the DLL becomes unstable.